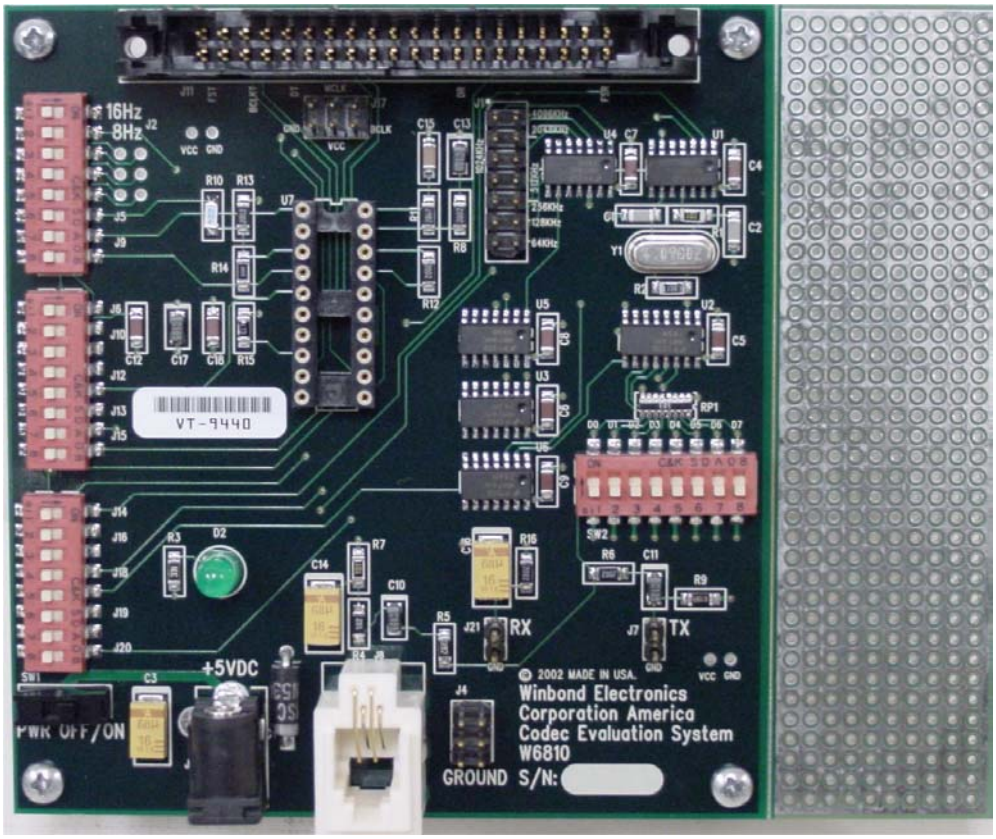
Winbond W6810, W681310 W681360, W681512, W681513 and W6811 CODEC Evaluation System User's Guide

W681xxx DK Evaluation Board Rev 6.12



WECA
2727 N First Street, San Jose CA 95134

Chapter - 1

Products supported by the W681xxx DK:

Part Number	# of Channels	PCM Format	Supply Voltage	Power (Typ/Stby)	Package
W6810	1	-Law / A-Law	**5V**	25mW / 0.5W	PDIP20
W6811	1	-Law / A-Law	**5V** Analog 3V Digital	25mW / 0.5W	PDIP24,
W681310	1	-Law / A-Law	3V	10mW / 0.5W	Via SOP20, SSOP20, To PDIP Converter
W681360	1	13-bit Linear	3V	9.8mW / 0.09W	Via SOP20, SSOP20, To PDIP Converter
W681511	1	-Law / A-Law	**5V**	25mW / 0.5W	Via SOP20 To PDIP Converter
W681512	1	-Law / A-Law	**5V**	30mW / 0.5W	Via SOP20, SSOP20, To PDIP Converter
W681513	1	-Law / A-Law	**5V**	25mW / 0.5W	Via SOP20 To PDIP Converter

W6810 Features

• Single +5 VDC power supply
• Typical power dissipation of 25 mW, power-down mode of 0.5 µW
• Fully-differential analog circuit design
• On-chip precision reference of 1.575 V for a 0 dBm 0TLP at 600Ω.
• Push-pull power amplifiers with external gain adjustment with 300Ω load capability
• Seven master clock rates of 256 kHz to 4.096 MHz
• Pin-selectable µ-Law and A-Law companding compliant with ITU G.711
• CODEC A/D and D/A filtering compliant with ITU G.712
• Pin1= Vref
• Pin2= RO-

W681511 Features:

• Single +5 VDC power supply
• Typical power dissipation of 25 mW, power-down mode of 0.5 µW
• Fully-differential analog circuit design
• On-chip precision reference of 1.575 V for a 0 dBm 0TLP at 600 Ω.
• Push-pull power amplifiers with external gain adjustment with 300Ω load capability
• Seven master clock rates of 256 kHz to 4.096 MHz
• Pin-selectable µ-Law and A-Law companding compliant with ITU G.711
• CODEC A/D and D/A filtering compliant with ITU G.712
• Pin1= RO+
• Pin2= NC

W6811 Features:

• Power supply:
  Analog 4.5 – 5.5 VDC
  Digital 2.7 – 3.3 VDC
• Typical power dissipation of 25 mW, power-down mode of 0.5 µW
• Fully-differential analog circuit design
• On-chip precision reference of 1.575 V for a 0 dBm 0TLP at 600Ω.
• Push-pull power amplifiers with external gain adjustment with 300Ω load capability
• Seven master clock rates of 256 kHz to 4.096 MHz
• Pin-selectable µ-Law and A-Law companding compliant with ITU G.711
• CODEC A/D and D/A filtering compliant with ITU G.712
• Pin1= Vref
• Pin2 = RO-

W681310 Features

• Single +3 VDC power supply
• Typical power dissipation of 25 mW, power-down mode of 0.5 µW
• Fully-differential analog circuit design
• On-chip precision reference of 1.575 V for a -5.0 dBm 0TLP at 600Ω.
• Push-pull power amplifiers with external gain adjustment with 300Ω load capability
• Seven master clock rates of 256 kHz to 4.096 MHz
• Pin-selectable µ-Law and A-Law companding compliant with ITU G.711
• CODEC A/D and D/A filtering compliant with ITU G.712
• Pin1= Vref
• Pin2= RO-

W681360 Features:

- 13-bit Linear ADC/DAC with 2's complement data format
- 3 VDC Power supply
- Low power consumption with active, power-saving and power-down modes
- Multiple Master clocks from 256 kHz to 4096 kHz
- Fully–Differential Analog Circuit Design for Lowest Noise
- Two PCM Digital Interface Clock Formats
- Short Frame Sync, Long Frame Sync
- On-Chip Precision Ref Voltage 0.886 V for a – 5.0 dBm 0TLP at 600Ω.
- Receive Gain Control from 0 dB to – 21 dB in 3 dB Steps.
- Industrial Temperature Range: (–40°C to +85°C)
- Pin16 = HB (High–Pass Filter Bypass)
- Pin1 = VAG Ref

W681513 FEATURES

• Single +5 VDC power supply
• Typical power dissipation of 30 mW, power-down mode of 0.5 µW
• Fully-differential analog circuit design
• On-chip precision reference of 1.575 V for a 0 dBm TLP at 600Ω.
• Push-pull power amplifiers with external gain adjustment with 300Ω load capability
• **Master clock rate supports 2.000 MHz** clock for USB applications
(See instructions on modification on pages 21, 22, and 23.)
• Pin-selectable µ-Law and A-Law companding compliant with ITU G.711
• CODEC A/D and D/A filtering compliant with ITU G.712
• Industrial temperature range (–40°C to +85°C)
• Package: 20-pin SOP (SOG)

General Description

Winbond's W681XXXDK Evaluation/Development System is a Stand-Alone unit that serves as a simple, easy-to-use demonstration board as well as a powerful evaluation system. All the functions of the W6810/W681310/ W681360 PCM CODECs may be selected in real time to allow complete evaluation of these ICs for an end application. The hardware includes many useful connectors that will allow easy connection to external hardware for use as an evaluation tool. Please use U7 socket for inserting supplied samples if not installed already at the factory.

Introduction:

The W6810, W681310, W681360, and W681315 are members of the W681XXX family of PCM CODECs. These CMOS products are single voice band CODECs. The CODECs comply with the specifications of the ITU-T G.712 recommendation. The W6810/W681310 also include a complete μ-Law and A-Law compander. The μ-Law and A-Law companders are designed to comply with the specifications of the ITU-T G.711 recommendation. The system can work at 256 kHz, 512 kHz, 1536 kHz, 1544 kHz, 2048 kHz, 2560 kHz & 4096 kHz clock rates. The system clock is supplied through the master clock input and can be derived from the bit-clock if desired.

User I/O to the W681XXXDK Evaluation board is provided via a number of connectors. These connectors are:

- A 40-pin header provides access to W681xxx analog and digital signals (J11)
- RJ9 handset jack (J8)
- Analog transmit and receive path headers (J7, J21)

W681xxxDK Features:

Easy to use (a stand-alone evaluation system)

- Single +5 VDC power supply (not supplied)
- Single +3 VDC Power Supply (not supplied) for W6811 or W681310/W681360
- Prototype area for application development
- Useful connectors for connecting to standard test equipment
- RJ9 jack for standard handset

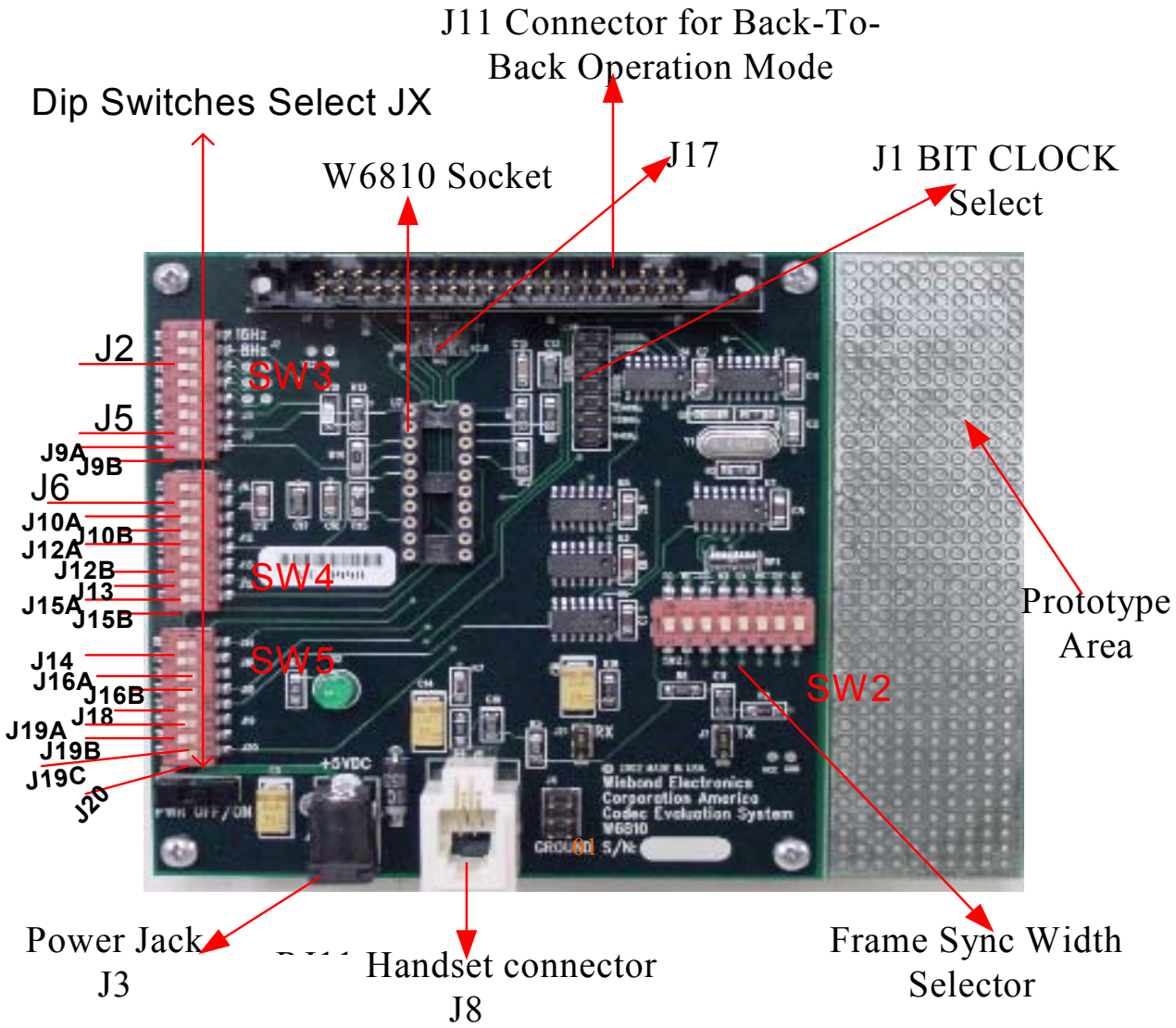


Figure 1: W681xxxDK Evaluation System Component Placement

Chapter - 2

Hardware Description

Clock Generator:

All the necessary clock rates such as Frame Sync, Bit Clock and the 256 KHz for the W681xxxDK evaluation system are driven from a single 4.096 MHz crystal oscillator.

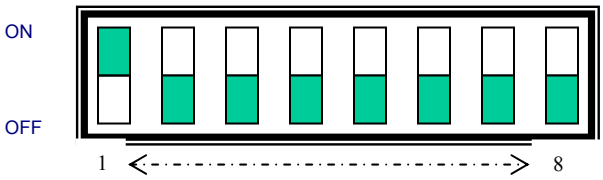
Frame Sync:

The Frame Sync is generated on the W681xxxDK evaluation board. J19 and J20 (SW5) control the FSR (Frame Sync Receive) and FSX (Frame Sync Transmit) routing. Enabling these jumpers also routes the signal to the 40-pin header (J11).
Setting Dip Switches:
Switch SW2 selects the width of the Frame Sync. The pulse width is set as a number of BCLKs. The following number of BCLKs for Frame Sync can be set with SW2.

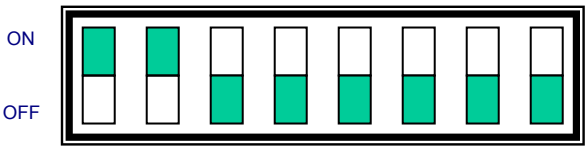
- 1-2-3-4-5-6-7-8

The Dip-Switch SW2 configurations are:

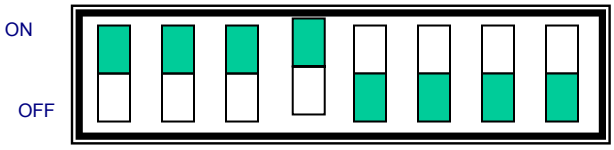
Frame Sync = 7 BCLK



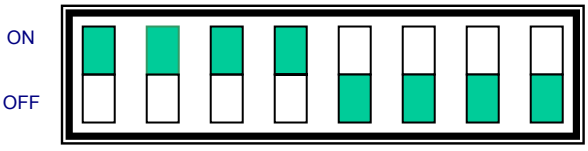
Frame Sync = 6 BCLK



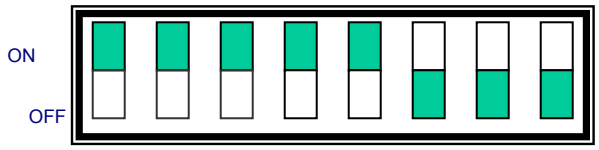
Frame Sync = 5 BCLK



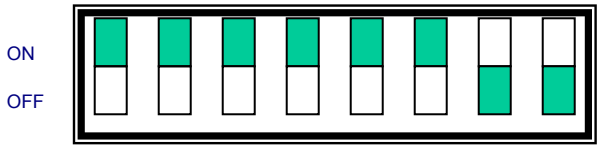
Frame Sync = 4 BCLK



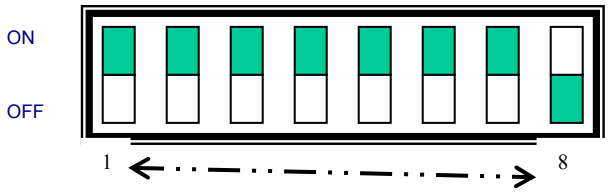
Frame Sync = 3 BCLK



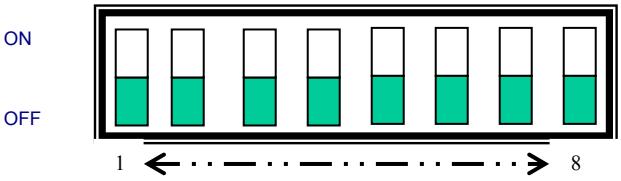
Frame Sync = 2 BCLK



Frame Sync = 1



Frame Sync = 8



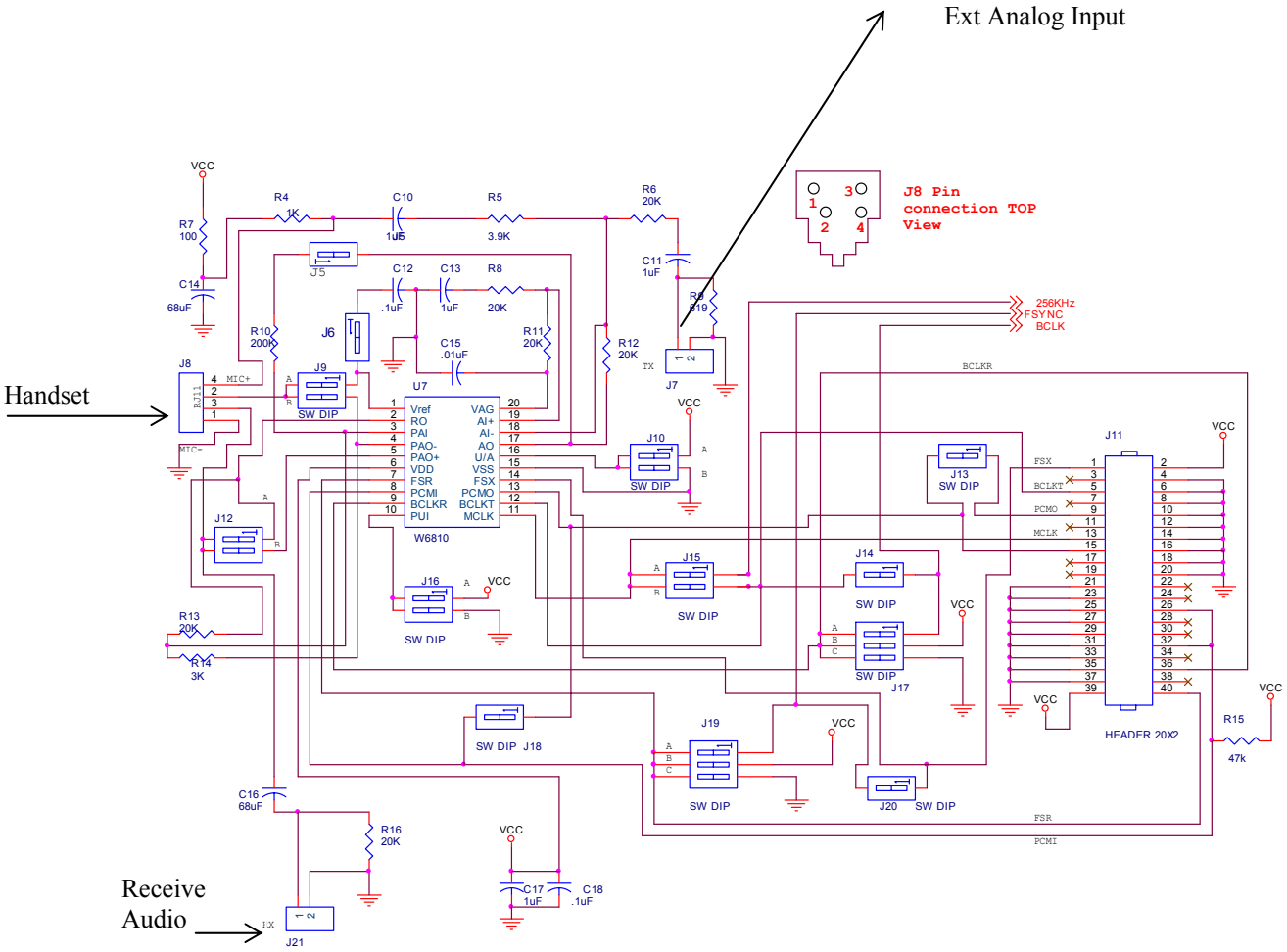
BIT CLOCK:

Bit clock is routed to the 2x20 (J11) header connector pins 5 (BCLKT) and 36 (BCLKR) through J17A and J14. J1 is used to select the frequency at which Bit Clock operates. The selected frequencies are 4.096 MHz, 2.048 MHz, 1.024 MHz, 512 KHz, 256 KHz, 128 KHz and 64 KHz.

256 KHZ: MCLK

The 256 KHz is a possible frequency setting for the master clock (MCLK) J15A (SW4) input on the chosen PCM CODEC-filter. J15B will configure the MCLK input to have a frequency equal to Bit Clock.

Figure 2: W681xxxDK Evaluation System Schematic Diagram



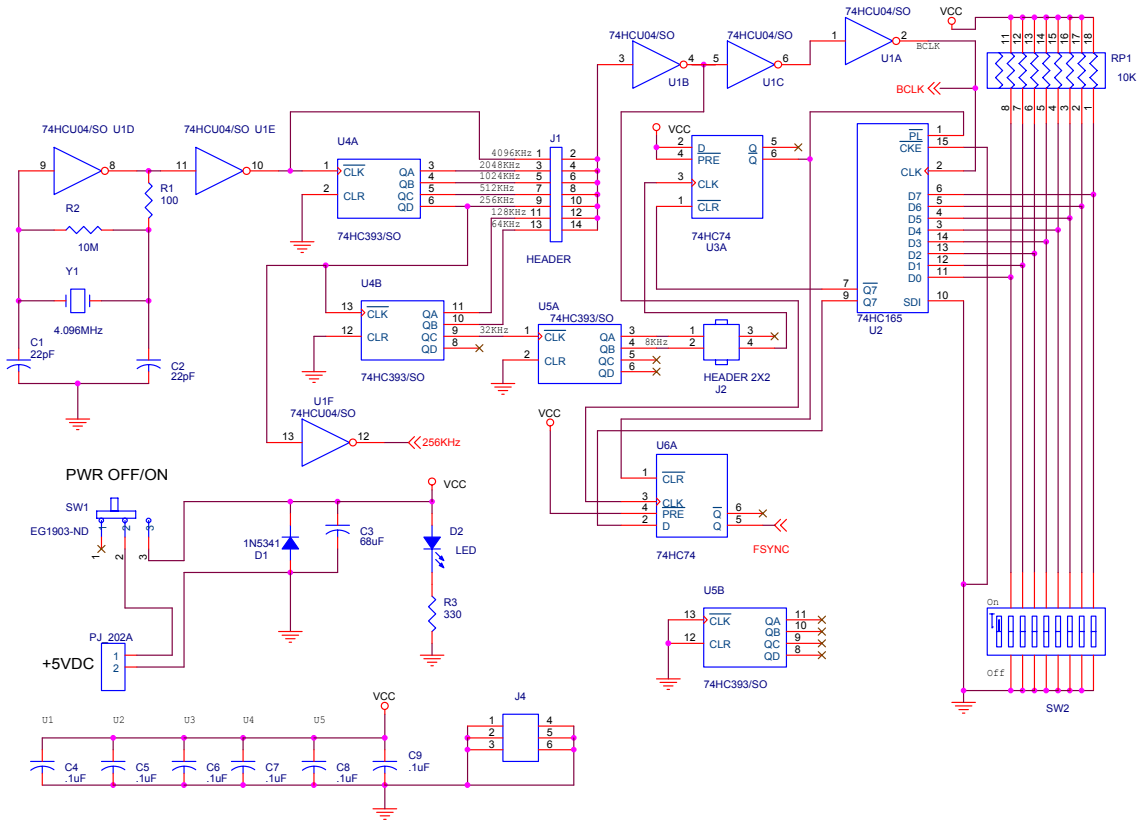


Figure 3: W681xxxDK Evaluation System Schematic Diagram:

Chapter – 3

Jumper Descriptions

DIP switches on the left hand side of the evaluation system are used to select a particular jumper. When a Jumper is populated (switch is Closed), it enables the function; an unpopulated Jumper (Open Switch) disables the function. The Jumpers are referenced as letters; for example J7A, J7B. Only one Jumper is closed for a selected function, not both, or the power supply can be shorted!

W6810DK JUMPERS/DIP SWITCHES FOR W6810

DIP SWITCH NUMBERS	JUMPER NAME	PURPOSE or FUNCTION	NOTES	u-Law Loopback No SideT	ISDN GCI Loopback B1/B2
SW3-1	J2A	16 KHz Sync N/C	Not Avail	0	0
-2	J2B	8 KHz Sync	Standard	1	1
-3	N/U			0	0
-4	N/U			0	0
-5	N/U			0	0
-6	J5	Sidetone Enable	Off	0	0
-7	J9A	Spkr to Vref		0	0
-8	J9B	Spkr to PAO-		1	1
SW4-1	J6	Vref cap enable	C12	1	1
-2	J10A	u-Law Select		1	1
-3	J10B	A-Law Select		0	0
-4	J12A	Spkr to RO-		0	0
-5	J12B	Spkr to PAO+		1	1
-6	J13	PCMT to J11-9		0	0
-7	J15A	MCLK to 256 Khz		0	0
-8	J15B	MCLK to BCLK		1	1
SW5-1	J14	BCLK to BCLKT		1	1
-2	JI6A	Power Up		1	1
-3	J16B	Power Down		0	0
-4	J18	Loopback Enable		1	1
-5	J19A	FSR to F Sync		1	0/0
-6	J19B	FSR to Vcc	B2 in GCI	0	0/1
-7	J19C	FSR to Gnd	B1 in GCI	0	1/0
-8	J20	FSX to F Sync		1	1
	J17A	BCLK = MCLK		√	
	J17B	Vcc			
	J17C	Gnd			√
	J1	BIT CLK SELECT		2048	2048

WARNING: Jumpers shaded in can short Vcc to Ground if set wrong.

Use +5 VDC Power Supply for this Chip.

W6810DK JUMPERS/DIP SWITCHES FOR W681360 LINEAR CODEC

DIP SWITCH NUMBERS	JUMPER NAME	PURPOSE or FUNCTION	NOTES	DIP Switch Settings
SW3-1	J2A	16 KHz Sync N/C	Not Avail	0
-2	J2B	8KHz Sync	Standard	1
-3	N/U			0
-4	N/U			0
-5	N/U			0
-6	J5	Sidetone Enable	Off/On	0/1
-7	J9A	Spkr to Vref		0
-8	J9B	Spkr to PAO-		1
SW4-1	J6	Vref cap enable	C12	1
-2	J10A	High Pass Off		0
-3	J10B	High Pass On		1
-4	J12A	Spkr to RO-		0
-5	J12B	Spkr to PAO+		1
-6	J13	PCMT to J11-9		1
-7	J15A	MCLK to 256 Khz		0
-8	J15B	MCLK to BCLK		1
SW5-1	J14	BCLK to BCLKT		1
-2	JI6A	Power Up		1
-3	J16B	Power Down		0
-4	J18	Loopback Enable		1
-5	J19A	FSR to F Sync		1
-6	J19B	FSR to Vcc		0
-7	J19C	FSR to Gnd		0
-8	J20	FSX to F Sync		1
	J17A	BCLK = MCLK		√
	J17B	Vcc		
	J17C	Gnd		
	J1	BIT CLK SELECT		2048 MHz

WARNING: Jumpers shaded can short Vcc to Ground if set wrong.

Use a +3 VDC Power Supply to board for this Demo.

W681512DK JUMPERS/DIP SWITCHES
FOR A-A, A-D, D-A TESTING

DIP SWITCH NUMBERS	JUMPER NAME	PURPOSE or FUNCTION	NOTES	A-A µ-Law Loopback No SideTone	PCM I/O W/ PCM-4 D/A-A/D
				On board clocks	External clocks
SW3-1	J2A	16KHz Sync N/C	Not Avail	0	0
-2	J2B	8KHz Sync	Standard	1	0
-3	N/U			0	0
-4	N/U			0	0
-5	N/U			0	0
-6	J5	Sidetone Enable	Off	0	0
-7	J9A	Spkr to Vref		0	0
-8	J9B	Spkr to PAO-		1	0
SW4-1	J6	Vref cap enable	C12	0	0
-2	J10A	u-Law Select		1	1
-3	J10B	A-Law Select		0	0
-4	J12A	Spkr to RO-		0	0
-5	J12B	Spkr to PAO+		1	1
-6	J13	PCMT to J11-9		0	1
-7	J15A	MCLK to 256Khz		0	0
-8	J15B	MCLK to BCLK		1	1
SW5-1	J14	BCLK to BCLKT		1	0
-2	JI6A	Power Up		1	1
-3	J16B	Power Down		0	0
-4	J18	Loopback Enable		1	0
-5	J19A	FSR to F Sync		1	0
-6	J19B	FSR to Vcc	B2 in GCI	0	0
-7	J19C	FSR to Gnd	B1 in GCI	0	0
-8	J20	FSX to F Sync		1	0
	J17A	BCLK = MCLK (right)		√	N/C
	J17B	Vcc (center)			N/C
	J17C	Gnd (left)			N/C
	J1	BIT CLK SELECT		2048	

WARNING: Jumpers shaded in Rose color can short Vcc to Ground if set wrong.

Use 5V Power. R!4 = 20K. 0TLP = 0.0 dBm.

PCM-4 General Parameter Settings

Parameter #	Selected	Details
1	11, 23	Digital Configuration
2	14, 24, 31	Frame Selection
3	13, 22, 31	Digital TX Interface
4	13, 22	Digital RX Interface
5	11,22	Digital Words in TX Frame
6	11	TX Error Insertion
7	12, 22 (11, 21)	Mu-Law or A-Law Select
8	11, 21	VF Input and Output #1
9	11, 13, 16, 22, 23, 27, 33, 35	Various Parameters
0	1 (3)	Plotter Selected (Printer)

Note: These settings will vary depending upon which Test from Table A or B is chosen when the Parameter button is pressed. This set of values is for A-A using the clocks from the PCM-4 to run the board. Used 4W Analog mode through PCMZ-4 with Switches On for DC isolation.

J1: Bit Clock Select:

J1 selects the Bit Clock frequencies from 4.096 MHz to 64 KHz.

J2A: Frame Sync:

J2A sets the Frame Sync (FSR) to 8 KHz (SW3-2)

J3: Power Supply Input Jack (5VDC or 3VDC) If you are evaluating a 5V product use 5VDC power supply. If you are evaluating a 3V product use a 3VDC power supply adapter with positive center.

J4: GND TST points

J5: Side Tone (SW3-6)

J5 enables the side tone path on the PCM CODEC filter

J6: VAG CAP ENABLE: (SW4-1)

J6 enables VAG filter cap

J7: Transmitter Audio Input

J8: RJ9 Handset connector.

J9A: 2.5V Reference Voltage (SW3-7)

J9A is not used.

J9B: SPKR+ = PAO (SW3-8)

J9B connects pin 4 W6810/W681310/W681360 to the RJ9 handset

J10: A-Law and µ-Law Selection or High-pass Bypass: (SW4-2) & (SW4-3)

J10A Selects µ-Law and J10B Selects A-Law for W6810/W6811/W681310/W681512. For W681360 J10 is used for High-pass Bypass. Determines if the transmit high-pass filter is used (HB='0') or bypassed (HB='1'). When the high-pass is bypassed the frequency response extends to DC.

J11: 2x20 pin Header:

This 40-pin header provides access to W6810/W681310/W681360 analog and digital signals for a user defined system, or a second W681xxxDK evaluation system for back-to-back operation.

J12A: SPKR- = R0- (SW4-4)

J12A connects RO- (Pin 2) to the RJ9 and the RX output connector.

J12B: SPKR-=PA0+ (SW4-5)

J12B connects PA0+ (Pin 5) to the RJ9 and the RX output connector.

J13: PCMT: (SW4-6)

J13 Connects the PCMT (PCM output W681xxx) to J11 (Pin 9).

J14: BCLKT=BCLK (SW5-1)

J14 connects BCLK to BCLKT (Pin 12) of the W6810/W681310 CODEC-Filter.

J15A: MCLK = 256 KHz (SW4-7)

J15A sets the MCLK (Pin 11) to 256 KHz.

J15B: MCLK=BCLK (SW4-8)

J15B sets the MCLK (Pin 11) to be equal to BCLK.

J16A: POWER-UP (SW5-2)

J16A connects the PUI (Pin 10) of the W6810/W681310 CODEC to VCC to power up the device.

J16B: POWER-Down (SW5-3)

J16B connects the PUI (Pin 10) of the W6810/W681310 CODEC to GND to power down the device.

J17A: BCLKR = BCLK

J17A connects BCLKR (Pin 9) of the PCM W6810/W681310/W681310 CODEC to BCLK.

J17B: BCLKR = GND

J17B connects BCLKR (Pin 9) of the PCM W6810/W681310 CODEC to VCC.

J17C: BCLKR = VCC

J17C Connects BCLKR (Pin 9) of the PCM W6810/W681310 CODEC to Ground

J18: PCMT = PCMR (SW5-4) LOOPBACK

J18 Connects PCM output data transmit (Pin 13) to PCM input data receive (Pin 8) of the W6810/W681310 CODEC.

J19A: FSR = FSYNC (SW5-5) SELECT NORMAL MODE

J19A connects FSR (Pin 7) of the W6810/W681310 CODEC to Frame Sync.

J19B: FSR = VCC (SW5-6) SELECT B2 IN GCI ISDN MODE

J19B connects FSR (Pin 7) of the W6810/W681310 CODEC to VCC.

J19C: FSR = GND (SW5-7) SELECT B1 IN GCI ISDN MODE

J19C connects FSR (Pin 7) of the W6810/W681310 CODEC to Ground.

J20: FSX= FSYNC (SW5-8)

J20 connects the on board generated Frame Sync to W6810/W681310 FSX (Pin 14) as well as to Pin 1 of the J11.

J21: Receiver Path OUTPUT

J21 can be connected to test equipment for measurements.

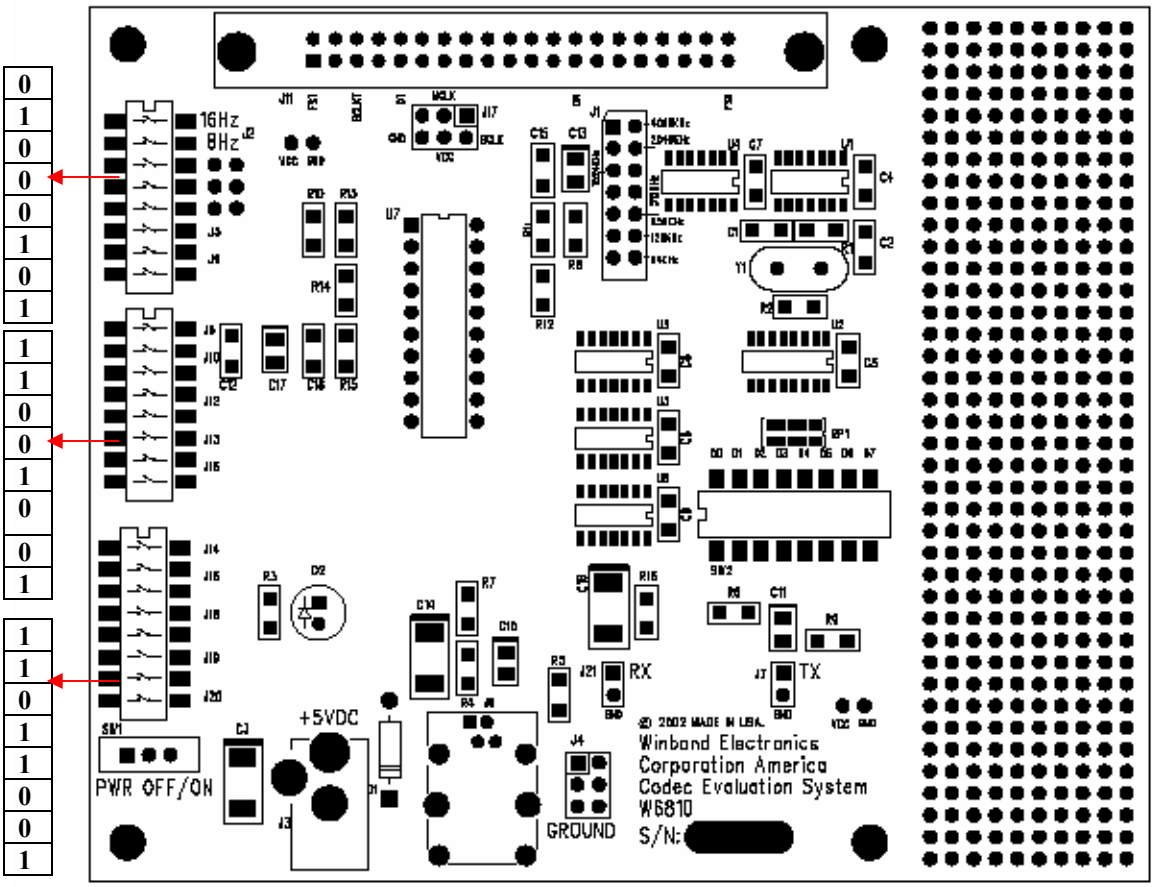
Chapter - 4

Operation Modes

The W681xxx-DK operates in two modes, Standalone and Back-To-Back mode.

Standalone Operation:

In this mode of operation the analog signal input at Transmit input (J7), is presented to the encoder of the W6810/W681310/W681360, where it is digitized and output on the PCM data transmit pin (13). Connecting J18 provides a local loop back to the PCM data input receive pin (PCMR) of the W6810/W681310, where it is reconstructed and output at J12 to J21 (RX). The following Jumpers are enabled in this mode J1 (2.048 MHz), J17A and J20. The DIP switches are set as follows.



J17 is enabled in the “A” position which is MCLK = BCLK

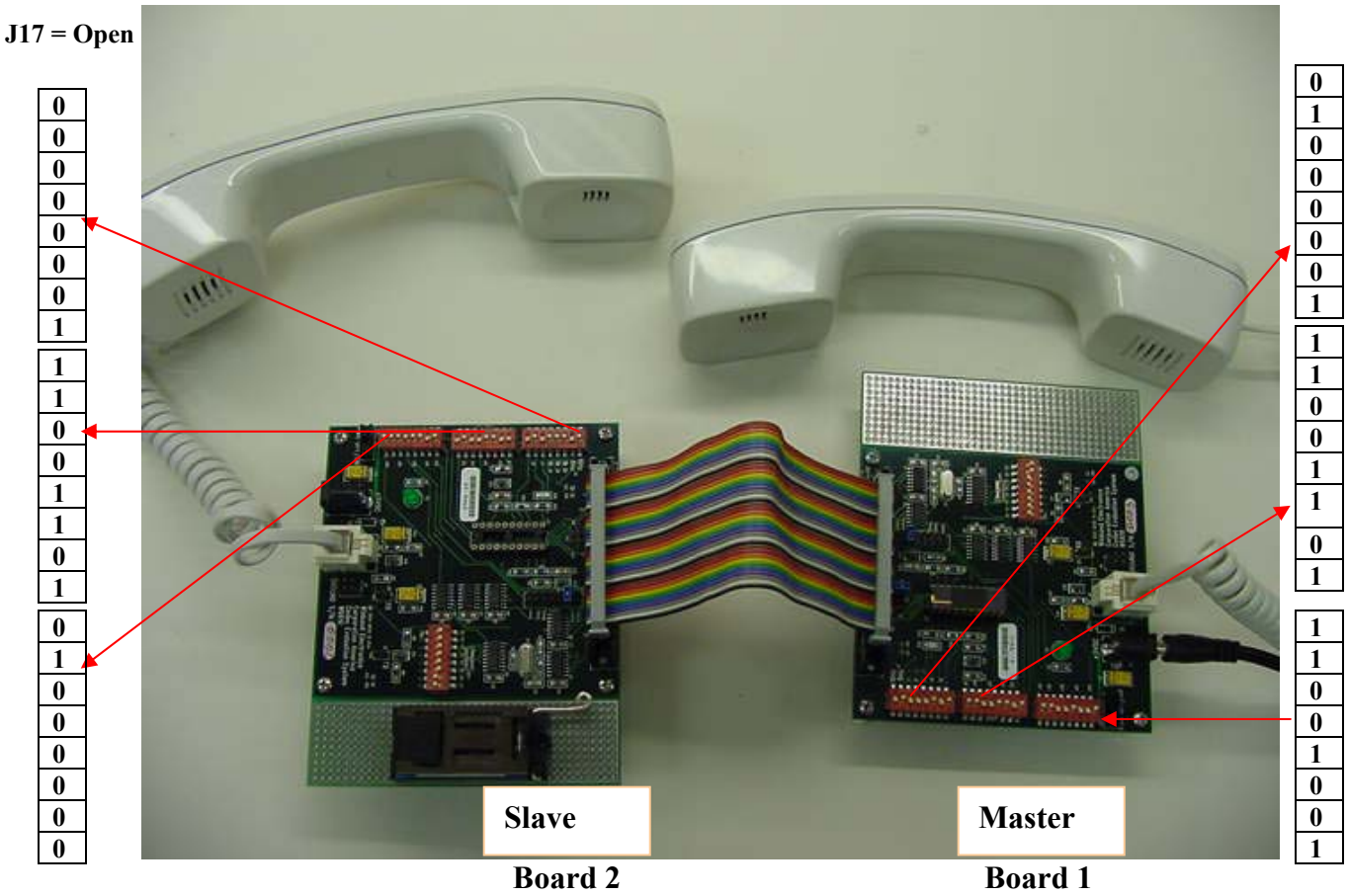
Back-To-Back Operation:

The W681XXXDK evaluation systems can be connected back to back using the 20x2 header (J11) .The cable should be maximum 2-3 inches in length. It makes all necessary electrical connections, allowing a full "analog-to-analog, "handset-to-handset" path to be established.

For back- to-back operation the jumper setting are set to ON position as follows for (W681XXXDK #1 Master board) unit. J1 (2.048 MHz), J2B, J5 (side tone), J9B, J6, J10A, J7A (for input).J12B, J13, J15B, J14, J16A, J19A and J20. The W681XXXDK #1 acts as the system master, providing BCLK and FSYNC to W681XXXDK #2. The jumper setting for board #2 is as follows. J1 (2.048 MHz), J2B, J5, J9B, J6, J10A J12B, J13, J15B and J16A.

The following DIP-switches are set as for back-to-back -mode

Note: Do not connect the power supply to the second board. It will be bussed to the second board through the 2x20 cable. Make sure the cable is connected as shown below.



W6810DK JUMPERS/DIP SWITCHES

FOR W6810 BACK-TO-BACK TEST

DIP SWITCH NUMBERS	JUMPER NAME	PURPOSE or FUNCTION	NOTES	SLAVE 2	MASTER 1 u-Law No SideTn
SW3-1	J2A	16 KHz Sync N/C	Not Avail	0	0
-2	J2B	8 KHz Sync	Standard	0	1
-3	N/U			0	0
-4	N/U			0	0
-5	N/U			0	0
-6	J5	Sidetone Enable	Off	0	0
-7	J9A	Spkr to Vref		0	0
-8	J9B	Spkr to PAO-		1	1
SW4-1	J6	Vref cap enable	C12	1	1
-2	J10A	u-Law Select		1	1
-3	J10B	A-Law Select		0	0
-4	J12A	Spkr to RO-		0	0
-5	J12B	Spkr to PAO+		1	1
-6	J13	PCMT to J11-9		1	1
-7	J15A	MCLK to 256 Khz		0	0
-8	J15B	MCLK to BCLK		1	1
SW5-1	J14	BCLK to BCLKT		0	1
-2	JI6A	Power Up		1	1
-3	J16B	Power Down		0	0
-4	J18	Loopback Enable		0	0
-5	J19A	FSR to F Sync		0	1
-6	J19B	FSR to Vcc	B2 in GCI	0	0
-7	J19C	FSR to Gnd	B1 in GCI	0	0
-8	J20	FSX to F Sync		0	1
	J17A	BCLK = MCLK		All Open	√
	J17B	Vcc			
	J17C	Gnd			
	J1	BIT CLK SELECT		2048 MHz	2048 MHz

WARNING: Jumpers shaded can short Vcc to Ground if set wrong.

Use a single 5 VDC Power Supply to Master Board 1 for this Demo. 0TLP = 0.0 dBm

W6810/W681310 Conversion to W6811

The W6811 is a general-purpose single channel PCM CODEC with pin-selectable μ-Law or A-Law companding. The device is compliant with the ITU G.712 specification. It operates from separate analog (5V) and digital (3V) power supplies. Functions performed include digitization and reconstruction of voice signals, and band limiting and smoothing filters required for PCM systems. The filters are compliant with ITU G.712 specification. The W6811 includes an on-chip precision voltage reference and an additional power amplifier capable of driving 300Ω loads differentially up to a level of 6.3V peak-to-peak. The analog section is fully differential, reducing noise and improving the power supply rejection ratio.

For evaluation of the W6811, use the W681XXXDK prototype area to wire up the W6811 to W6810/W681310 socket (U7 on the board) as shown below in Figure 1(If it is desired to connect a separate 3V power supply for digital I/O) otherwise use the direct connection below in Figure 2.

Note: The MC74HCLVX parts are only level translators in this application board. Please make sure the Analog power is applied first and then the digital power for part to function properly.

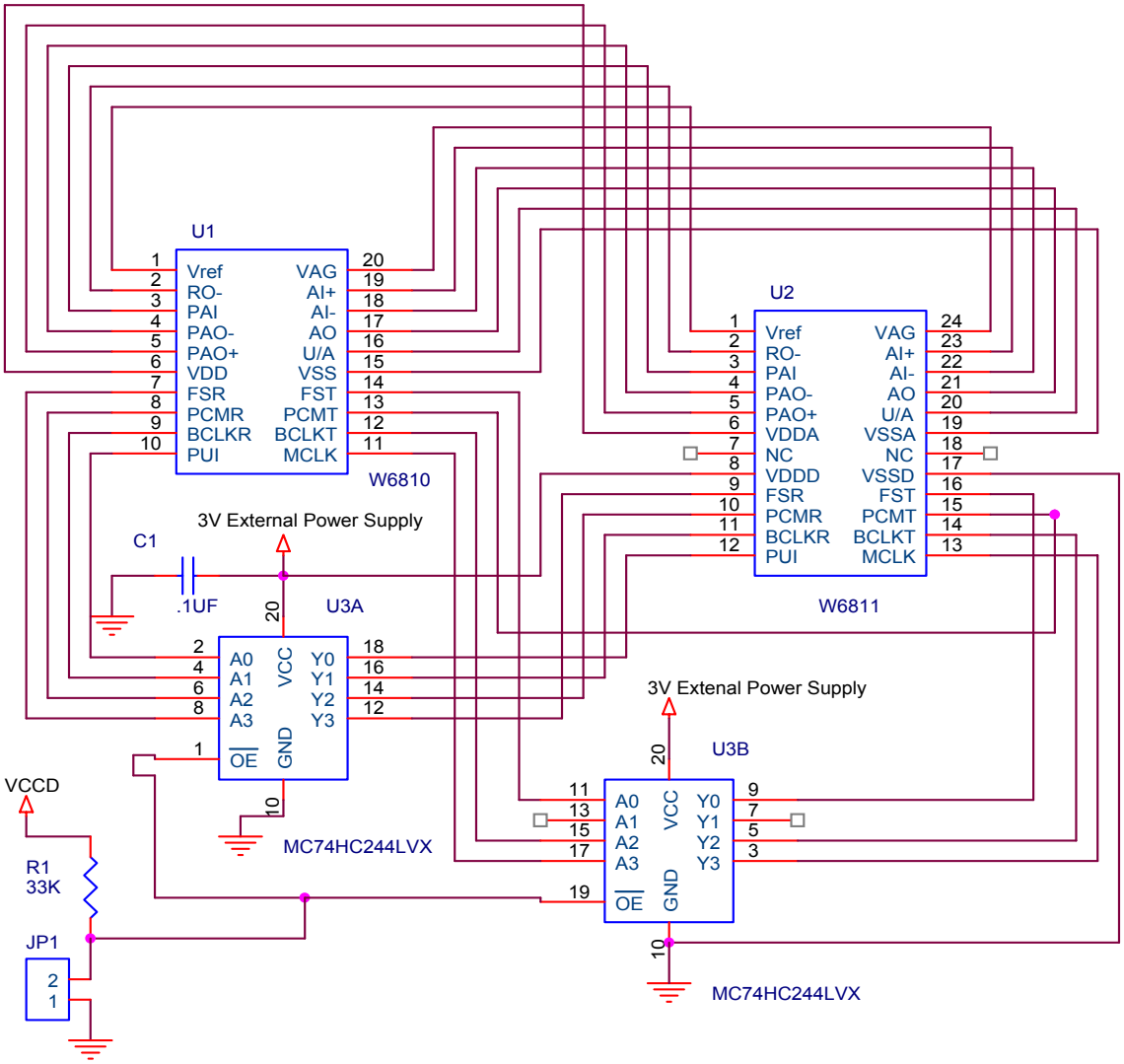


Figure 1

For performance evaluation of the W6811 with 5 VDC Digital I/O (the device works similar to W6810/W681310) you can connect the W6810/W681310 Socket on the W681XXXDK to a prototype board which has the W6811 foot print as below in Figure 2.

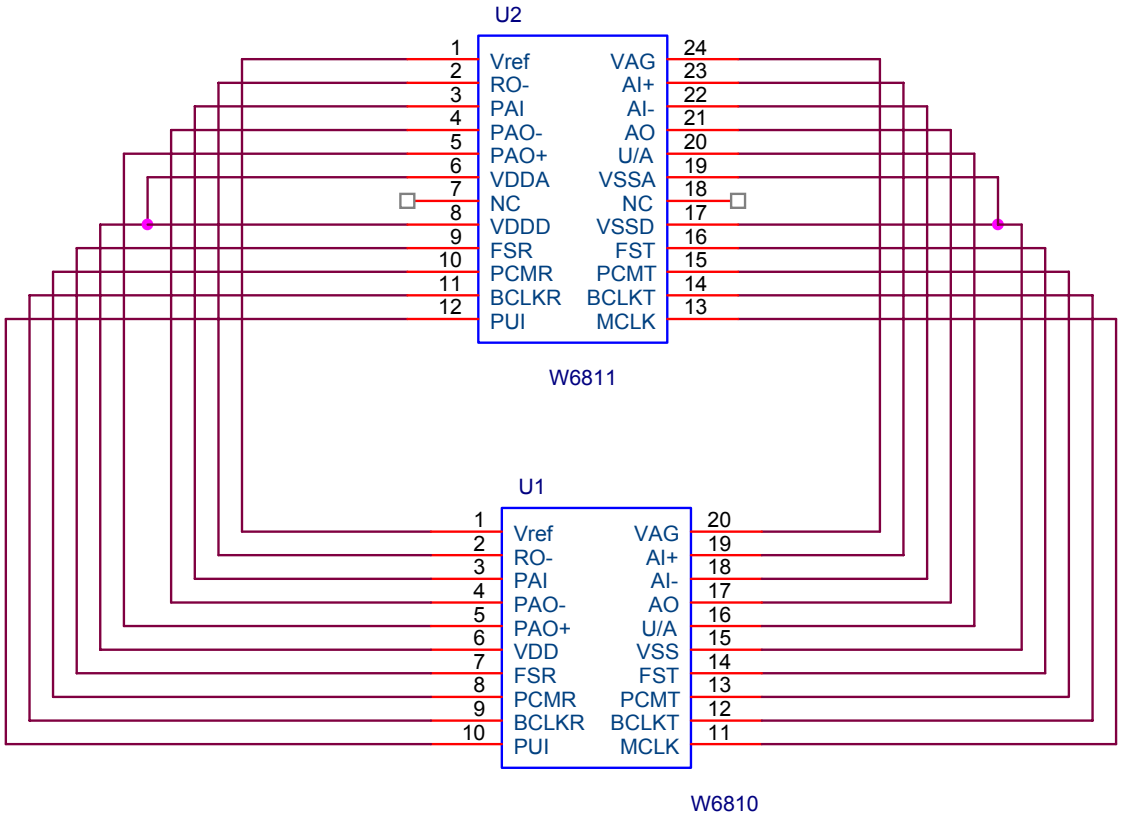
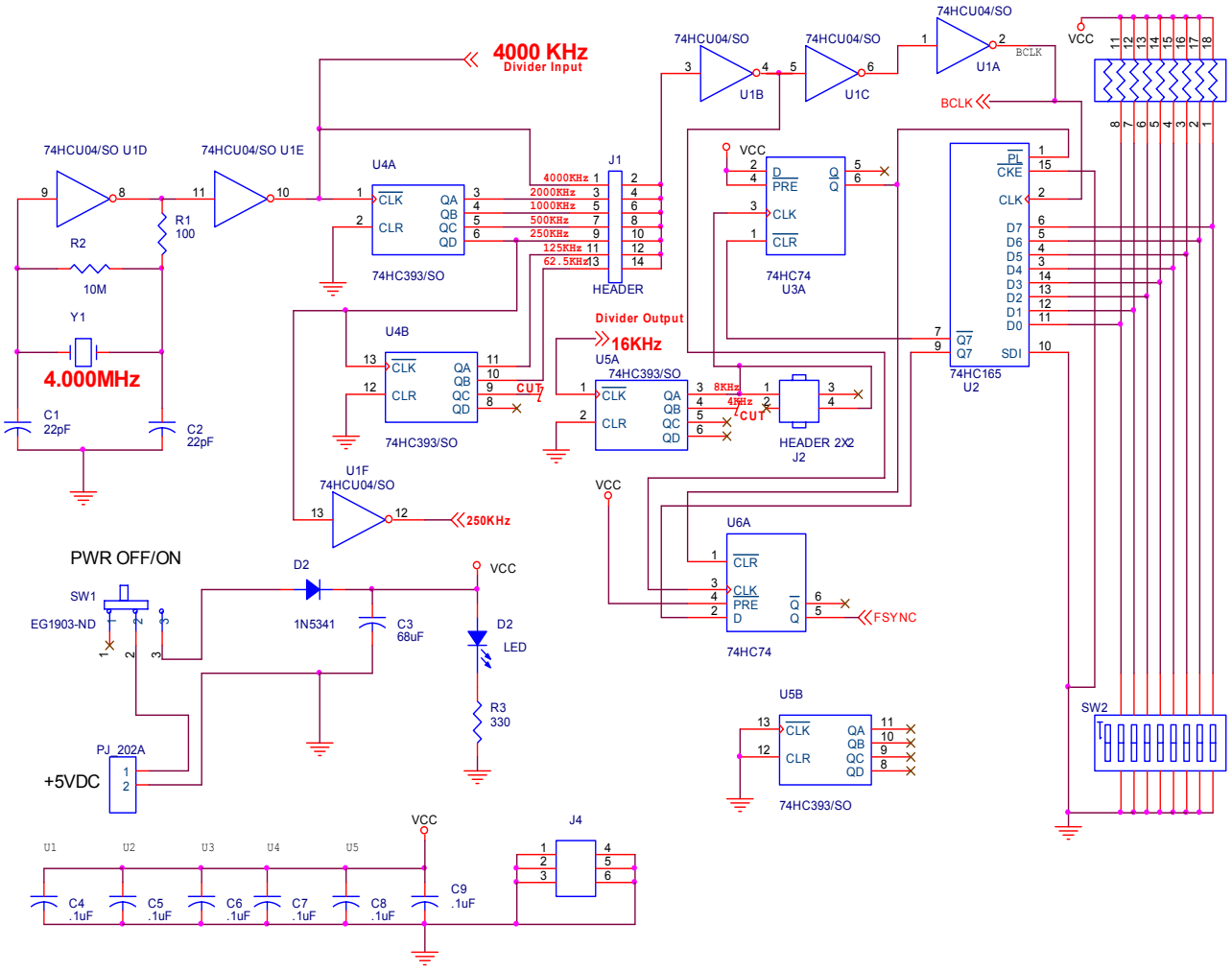


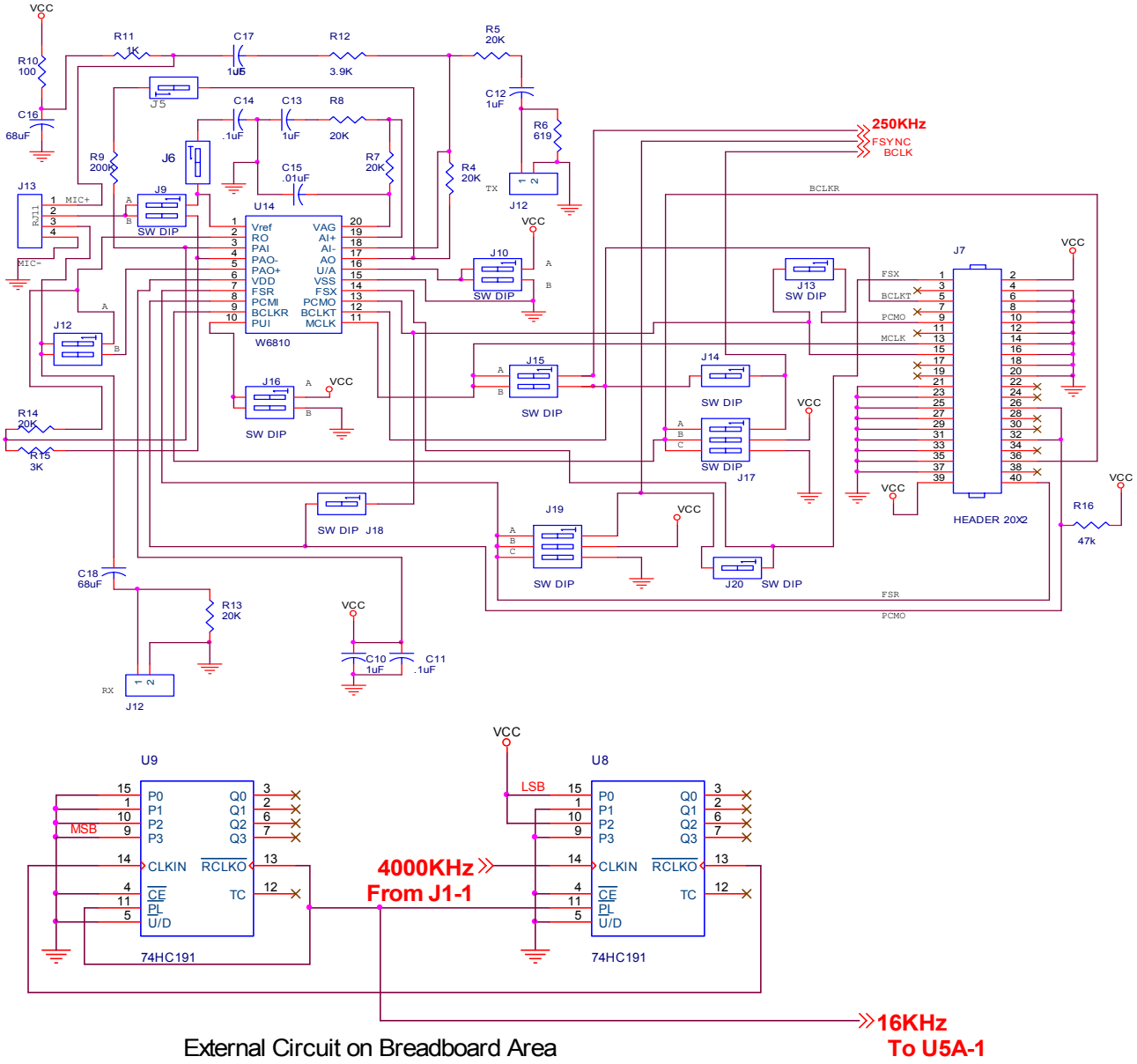
Figure 2

W6810/W681310 Conversion to W681513

The W6810DK has to be modified to allow the demonstration of the W681513 because of the 2.000 MHz clock rather than the 2.048 MHz standard frequency. The W681xxx-DK board is designed to divide 2048 KHz by 256 to get the 8 KHz sample clock. For the W681513 we substitute a 4.000 MHz crystal on the board and then build an external divider to do the divide by 250 to get 8 KHz again. It is a fairly simple modification requiring the addition of two divider chips on the prototyping area of the board. Follow these steps.

1. Change Y1 to 4.000 MHz.
2. Make Cuts at U4-9 and U5-4.
3. Add Jumper connecting U5-3 to U3-3.
4. Add Ripple counter circuit (See below external circuit on the bread board area) to breadboard area and connect as shown.


4000 KHz
Divider Input
74HCU04/SO U1D
74HCU04/SO U1E
74HCU04/SO
U1A
U1B
U1C
BCLK
VCC
U4A
74HC393/SO
J1
HEADER
4000KHz
2000KHz
1000KHz
500KHz
250KHz
125KHz
62.5KHz
R1
100
R2
10M
Y1
4.000MHz
C1
22pF
C2
22pF
U4B
CUT
Divider Output
16KHz
U5A
8KHz
4KHz
HEADER 2X2
J2
74HC74
U3A
74HC165
U2
U1F
250KHz
PWR OFF/ON
SW1
EG1903-ND
D2
1N5341
C3
68uF
LED
R3
330
PJ 202A
+5VDC
U6A
FSYNC
U5B
SW2
J4
C4 .1uF
C5 .1uF
C6 .1uF
C7 .1uF
C8 .1uF
C9 .1uF



External Circuit on Breadboard Area

Calculation:
Divide by 251 counter; Data = 256 - 251 = 5
Binary 5 = 00000101 0000 @ U9; 0101 @ U8

Table below describes the various CODEC support on the W681xxxDK Systems.

Evaluation Board part Number	Winbond CODEC Part number
W6810 DK	W6810/ W6811
W681512DK	W681512
W681310DK	W681310
W681360DK	W681360

W681xxxDK Part Number

The information contained in this datasheet may be subject to change without notice. It is the responsibility of the customer to check the Winbond USA website (www.winbond-usa.com) periodically for the latest version of this document, and any Errata Sheets that may be generated

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